REMARKS

This application has been reviewed in light of the Final Office Action mailed October 31, 2005. Reconsideration of this application in view of the below remarks is respectfully requested. Claims 1-38 are pending in the application with Claims 5-20, 25-29, 31 and 33-36 having been withdrawn. Of the presently elected claims, Claim 1 is in independent form. By the present amendment, Claim 1 has been amended. No new subject matter has been introduced by way of the present amendment.

Initially, the Examiner's attention is brought to previously presented Claims 37 and 38. These claims were newly added in the Amendment dated September 20, 2005. However, due to an over-sight on the Examiner's part, Claims 37 and 38 have not, as of yet, been considered. Therefore, Applicant respectfully requests withdrawal of the finality of the present Office Action and consideration of the claims, including Claims 37 and 38, and the remarks below as presently submitted.

I. Rejection of Claims 1 and 2 Under 35 U.S.C. § 102(b)

Claims 1 and 2 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,524,114 issued to Peng.

Claim 1 has been amended to recite: "...said two-pulse generator comprises a gate signal generator for generating a gate signal to extract two pulses from said test clock and a latch gate circuit for outputting two pulses from said test clock according to said gate signal, said gate signal generator generating said gate signal after a predetermined interval after an edge of said test clock signal as measured from an input timing of a control signal."

Since FIG. 3 of Peng clearly shows that the gate signal (SCK-1) 222 is synchronized with the test clock (TCK) 110, such that the rising edge of SCK-1 222 occurs simultaneous with the

rising edge of TCK 110, Peng fails to teach outputting two pulses from said test clock according to said gate signal, said gate signal generator generating said gate signal after a predetermined interval after an edge of said test clock signal as measured from an input timing of a control signal. Further, Peng discloses that clock pulses 312 of SCK-1 222 and 316 of TCK 110 are phase locked in frequency and phase. Therefore, each clock pulse leading edge, when going from a logic low to a logic high, will occur at substantially the same time. (See: FIG. 3 312, 316, and 318; col. 7, lines 45-50). Consequently, Peng does not teach generating the gate signal after a predetermined interval after an edge of the test clock signal.

Therefore, for at least the reasons given above, Claims 1 and 2 are believed to patentably distinct and allowable over the prior art references. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claims 1 and 2 under 35 U.S.C. § 102(b).

II. Rejection of Claims 3-4, 21-24, 30 and 32 Under 35 U.S.C. § 103(a)

Claims 3-4, 21-24, 30 and 32 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentably obvious over Peng in view of U.S. Patent No. 5,794,175 issued to Conner. Claims 3-4, 21-24, 30 and 32 depend from independent Claim 1 and thus recite all the limitations of that independent claim.

While Conner discloses a printed circuit board (PCB) memory array board 210 having a plurality of sockets for burn-in quality testing, there is, however, no disclosure or suggestion of a delay test and two-pulse generator, wherein a gate signal generator generate a gate signal after a predetermined interval as measured from an input timing of a control signal, as recited in Applicant's independent Claim 1.

Regarding the rejection of Claims 4 and 30, the Examiner asserts that frequency divider 210 of Peng is equivalent to the claimed frequency multiplying PLL circuit by citing that

dividing a frequency by N is the equivalent of multiplying that same frequency by 1/N. However, while this is mathematically correct, the result is not equivalent since multiplying the frequency by 1/N will reduce the frequency. What is meant by "to multiply the frequency" as recited in the claim and supported throughout the specification is "to increase the frequency" by a given factor. Additionally, supporting circuitry would be necessary to allow an input of value N to produce a multiplied frequency output of (N*frequency) using a frequency divider 210, thus the frequency divider 210 and the frequency multiplying PLL cannot properly be equated.

Conner fails to overcome the above-identified deficiencies of Peng, and so Peng and Conner, taken alone or in any proper combination, fail to disclose or suggest the limitations recited in Applicant's Claim 1. Accordingly, for at least the reasons given above, Applicant respectfully requests withdrawal of the rejection with respect to Claims 3-4, 21-24, 30 and 32 under 35 U.S.C. § 103(a) over Peng in view of Conner.

III. Previously Presented Claims 37 and 38

Claims 37 and 38, reciting: "The test circuit according to claim 1, wherein said gate signal generator comprises a control circuit for adjusting a timing of said gate signal" and "The test circuit according to claim 37, wherein said control circuit counts said test clock for adjusting said timing of said gate signal" respectively, were added in the Amendment dated September 20, 2005. The limitations recited in these claims are supported in FIG. 3 and on page 2, paragraph 0040 through page 3, paragraph 0046. Accordingly, no new subject matter is introduced by way of Claims 37 and 38.

CONCLUSIONS

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-4, 21-24, 30, 32 and 37-38 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,

Paul J. Esatto, Jr.
Registration No. 30,749

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 Garden City Plaza - Ste. 300
Garden City, New York 11530
(516) 742-4343

PJE:DAT:jam